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Fault Tolerance of the Pulsed Power Circuit Architecture for the NIF

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Prefer poster session

Abstract

A simple circuit architecture is proposed for the NIF pulsed power system which results in reduced system costs compared with previous laser ICF facilities. The number of individual pulsed power modules is reduced by maximizing the energy delivered by each module. A compact and simplified layout reduces assembly, installation and overall facility costs. Minimizing the number of independent modules further reduces costs by reducing the number of controllers, charging supplies, switches, trigger generators, enclosures and other components whose cost is relatively insensitive to the module energy.

Although the proposed architecture is potentially very cost-effective, there are a number of technical issues which must be addressed the system can be deployed. Fault tolerance of the circuit and development of a suitable output switch are the most important of these. This paper addresses only the fault tolerance. The proposed architecture has 20 capacitors connected in parallel storing 1.6 MJ in each module. Any fault in the system has the potential of releasing this 1.6 MJ through the fault. The module must be designed so that the anticipated faults result in acceptable time and cost to repair the module. For example, lossy inductors in series with each capacitor are used to provide isolation in the event of an individual capacitor failure and to limit capacitor current to an acceptable level for bus or transmission line faults. System failure modes which must be accommodated in the design must also include a shorted flashlamp and an output switch pre-fire during or after capacitor charging.

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A 1.6 MJ pulsed power test-bed has been constructed in order to develop and validate solutions to these fault modes. A detailed transient circuit model, validated by data from test-bed experiments, is used to thoroughly explore the fault tolerance of the design. This paper describes the results to date of a program to identify these fault modes and accommodate them in the design. The circuit topology proposed for the NIF is described and is compared to that of previous systems. The transient circuit model and the test-bed capacitor bank are described. Data and analysis from capacitor faults, bus faults and flashlamp faults is given.